2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yasuyuki MORISHITA	Examiner:	Nadav, Ori
Serial No.:	09/621,614	Group Art Unit:	2811
Filed:	07/21/00	Docket:	040373-0287
Title:	SEMICONDUCTOR DEVICE		

CERTIFICATE OF MAILING

Commissioner for Patents
Washington, D.C. 20231

Sir:

I hereby certify that the following paper(s) and/or fee along with any attachments referred to or identified as being attached or enclosed are being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. § 1.8(a) on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, Washington D.C. 20231.

☒ Transmittal sheet in duplicate.
☒ Supplemental Information Disclosure Statement; Form PTO-1449; copies of references.
☒ Return receipt postcard.

Please charge any additional fees associated with this transmittal to Deposit Account No 19-0741. A duplicate of this sheet is enclosed.

Dated: February 7, 2002

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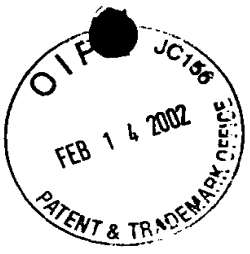

Atty. Dkt. No. 040373/0287

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#17
2-25-02
Dayton

Applicant: Yasuyuki MORISHITA

Title: SEMICONDUCTOR DEVICE

Appl. No.: 09/621,614

Filing Date: 07/21/00

Examiner: Nadav, Ori

Art Unit: 2811

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO-1449 is a listing of documents known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 C.F.R. 1.56. A copy of each listed document is being submitted to comply with the provisions of 37 C.F.R. 1.97 and 1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 C.F.R. §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a prima facie prior art reference against the claims of the present application.

CONCISE EXPLANATION OF
RELEVANCE OF EACH DOCUMENT

Pursuant to 37 C.F.R. §1.97(e)(1), the undersigned Attorney of record hereby states that each item of information contained in this Supplemental Information Disclosure Statement filed herewith was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Supplemental Information Disclosure Statement.

English translations of the Japanese documents are not readily available; however, English language abstracts are provided herewith. The absence of such translations does not relieve the PTO from its duty to consider the submitted documents (37 C.F.R. §1.98 and MPEP §609).

The U.S. patents listed below correspond to the following foreign patent applications in which they were cited.

U.S.	Foreign
5,898,206	JP 10-189756
6,015,992	JP 10-294430
5,572,394	JP 08-288403
5,581,103	JP 07-029987

The Japanese Examiner stated in connection with the corresponding application in Japan:

Ref# 40373/287 SN: 09/621614

1. The patent pertaining to the following claims of the submitted application is an invention that was described in the following publications, which had been distributed either in Japan or abroad prior to the submission of that application. For this reason, it cannot be awarded a patent based on the stipulations set forth in Article 29, Sections 1 and 3 of the Patent Law.

2. The patent pertaining to the following claims of the submitted application was based on an invention that was described in the following publications, which had been distributed either in Japan or abroad prior to the submission of that application. It could have easily been devised prior to the submission of the application by anyone with a normal level of technical knowledge of the field to which the invention belongs. For this reason, it cannot be awarded a patent based on the stipulations set forth in Article 29, Section 2 of the Patent Law.

Note (Refer to the List of Cited Literature regarding cited literature, etc.)

Regarding Claim 1
Reasons: 1, 2
Cited Literature: 1
Comments:

Cited Literature 1, and Figure 10 in particular, describe the invention of an input/output guard circuit that comprises a transistor made from an N^+-type diffused layer 3A (the No. 1 diffused layer in Claim 1), an N^+-type diffused layer 3Ba (corresponding to the No. 2 diffused layer in Claim 1), and an N^--type diffused layer 21a (corresponding to the No. 1 conductor-type well) under a P^+-type diffused layer 9C (corresponding to the No. 2 conductor-type impurity diffusion region in Claim 1) and an N^+-type diffused layer 3A.

Regarding Claim 2:
Reasons: 1, 2
Cited Literature: 1
Comments:

Cited Literature 1, and Figure 10 in particular, show a P^+-type diffusion layer 9C provided on top of a P-well 2A, where the bottom of said P-well 2A is at the same depth as the bottom of the aforementioned N^--type diffusion layer 21a.

Regarding Claim 3:
Reasons: 1, 2
Cited Literature: 1
Comments:

Cited Literature 1 describes the aforementioned transistor being an N-channel type transistor.

Regarding Claim 4:
Reasons: 1, 2
Cited Literature: 1
Comments:

Cited Literature 1, and Figure 10 in particular, describe the input/output guard circuit as being comprised of complementary transistors.

For what follows, refer to the comments for Claim 1.

Regarding Claim 5:
Reasons: 1, 2
Cited Literature: 1
Comments:

Refer to the comments for Claim 2.

Regarding Claim 6:
Reasons: 2
Cited Literature: 1, 2
Comments:

Cited Literature 2 discloses a technology wherein a high-concentration impurity region is provided under the well for the region in which a transistor is fabricated, doing so to prevent latch-up.

In Cited Literature 1 as well, the prevention of latch-up is a well-known technical issue, and when one considers the aforementioned problem, it would be easy for one skilled in the art to envision the use of the technology disclosed in the aforementioned Cited Literature 2 in the input/output guard circuit of Cited Literature 1.

Regarding Claim 7:
Reasons: 1, 2
Cited Literature: 1
Comments:

Refer to the comments listed for Claim 3.

List of Cited Literature

1. Japanese Unexamined Patent Application Publication H10-189756
2. Japanese Unexamined Patent Application Publication H09-321150

Record of Prior Art Literature Search Results

- Fields Searched IPC 7th Edition
  H01L 27/04
  H01L 27/08

- Prior Art Literature
  Japanese Unexamined Patent Application Publication H10-294430
  Japanese Unexamined Patent Application Publication H08-288403
  Japanese Unexamined Patent Application Publication H07-029987
  Japanese Unexamined Patent Application Publication H06-053420

This List of Prior Art Literature Search Results does not constitute a reason for rejection.

Applicant respectfully requests that the listed documents be considered by the Examiner and formally be made of record in the present application and that an initialed copy of Form PTO-1449 be returned in accordance with MPEP §609.

Respectfully submitted,

Date February 7, 2002

By 

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